Material aspects for batch integration of PZT thin films using transfer bonding technologies – Q2M development

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Abstract

Transfer bonding is a reliable cost-efficient and low-temperature CMOS compatible technique which allows batch integration of materials whose incompatibility with Si makes them unsuitable for monolithic integration. In this heterogeneous device integration method the material and process incompatibilities inherent in Si IC technology are overcome by fabricating devices on separate substrates and then transferring them onto target (e.g. CMOS) wafers. Transfer bonding has great potential for integrating RF-MEMS devices incorporating, for example, high thermal budget materials such as PZT and PST or non-ferroelectric piezoelectrics such as AlN and ZnO into microwave ICs for enhanced systems performance. This paper presents an overview of technology developments within the EU sponsored project Q2M for the realization of transfer bonded piezoelectrically actuated RF MEMS switches and other components focusing in particular on material factors relating to growth of the piezoelectric films, in this case sol-gel deposited PZT, that restricts the choice of device layers and impact on PZT properties such as microstructure, film orientation and piezoelectric coefficients. New process developments such as hard masking of PZT pattern during RIE etching and its compatibility with polymer transfer bonding are discussed.

Keywords: PZT, transfer bonding, RF MEMS switches, sol-gel

1. Introduction

If the recent drive to incorporate sensing and actuation functions into electronic circuits continues it will revolutionize the fields of microsystems and RF technology, particularly wireless communications and automotive electronics. The potential for integration of RF-MEMS components with well-established IC technology has already been demonstrated with realization of thin film bulk acoustic resonators (FBAR) duplexer filters for mobile phones [1]. There is now a current technological quest to develop reliable and cost-efficient batch integration techniques that provide for incorporation of high thermal budget materials such as PbZr\textsubscript{Ti}O\textsubscript{3} (PZT) and Pb\textsubscript{x}Sr\textsubscript{1-x}TiO\textsubscript{3} (PST) or non-ferroelectric piezoelectrics such as AlN and ZnO and so enable increased functionality and superior systems performance. Piezoelectric sensing/actuation offers advantages over alternatives such as high actuation force at low voltage and linear response with wide dynamic range [2] and among thin film piezoelectrics PZT has received most attention for MEMS applications as it has the highest piezoelectric coefficients and hence exhibits the best electromechanical performance. However, for some applications PZT’s high dielectric constant is a limitation as is its CMOS incompatible growth temperature and in these cases, AlN, in particular, is an attractive alternative which in addition to CMOS direct integration offers improved signal-to-noise ratio and high power efficiency [2].

As monolithic integration of PZT continues to prove elusive, new and alternative CMOS-compatible heterogeneous device integration methods have received great attention recently with the focus on novel transfer bonding techniques to overcome the material and process incompatibilities that arise when combining dissimilar materials. For example within the EU FP6 sponsored project Q2M [3], a consortium is currently investigating the suitability of a range of transfer bonding techniques for application specific RF-MEMS device integration incorporating PZT thin film actuators. This article gives an overview of the batch integration of PZT thin film devices onto dissimilar substrates, and consequent materials and process constraints applicable to two of the transfer techniques recently developed within the Q2M: wafer level microdevice distribution technology using selective transfer and adhesive full wafer transfer bonding [4,5]. The separation of the device processing onto different substrates, i.e. an auxiliary substrate and target RF substrates, and the transfer bonding between these substrates allow new possibilities to develop innovative actuator designs and fabrication processes. As an example, hard masking for RIE patterning of PZT is described in this paper.

2. PZT transducer stack – Microstructure design

The ideal PZT device structure consists of a PZT thin film sandwiched between two electrodes in direct contact with the substrate as shown in Fig.1. However, PZT film quality depends largely on control of interdiffusion and surface chemical reactions involving the layers that form the PZT composite [2,6] and for the sol-gel deposited films used in the present work it has been established that Pb from the sol diffuses through the bottom electrode into the substrate during the nucleation and growth of the perovskite PZT, and if for
example a standard Si substrate is used, forms lead silicates (PbSiO$_4$) that can cause delamination of the overlying electrode [6,7]. To avoid this, a barrier layer such as SiO$_2$, Si$_3$N$_4$ or TiO$_2$ must be inserted between the bottom electrode and the substrate to limit the diffusion of Pb and also to prevent formation of PtSi which would also have a deleterious effect.

Fig. 1. Schematic - an ideal PZT transducer stack

2.1. Device layer – Standard structure

Until recently most research studies have been concerned with obtaining high quality PZT films on Si with a standard structure composed of Pt/Ti bottom electrodes on top of a thermally grown SiO$_2$ barrier layer. In addition to Pb diffusion, which in fact, both these layers together prevent, other processes occur during PZT crystallization and these are depicted schematically in Fig. 2. The Ti which diffuses along grain boundaries to the Pt surface provides nucleation sites and the fleeting formation of an intermetallic phase, Pt$_3$Pb also influences perovskite phase transformation with the preferred PZT grain orientation [7]. As evident, material constraints imposed by the layers available for a specific device design means that the actual layer structures has to be more complex for practical applications. To make progress on novel device development, it is interesting to understand the material factors that influence the choice of layers and the consequent effect on PZT actuation properties.

Fig. 2. PZT device structures - schematic diagram of chemical interactions at layer interfaces

(a) Pb diffusion into the barrier causes cracks; (b) Pb diffusion into Pt and alloying (Pt$_3$Pb); (c) Ti diffusion to Pt surface provides nucleation sites; (d) diffusion of O$_2$ to Ti adhesion layer forming an oxide layer

3. Transfer bonding process – Layer design

As proposed within the Q2M project, two routes for transfer bonding technologies, already described in detail in our previous publications [4, 5], for realization of piezo-actuated RF switches are under development which requires PZT stacks with different types of layer structures for the different design configurations and process layouts under consideration. The choice of materials and process parameters is crucial to the successful implementation of transfer bonding with no degradation of PZT film quality.

While pursuing process layouts and overall device design, different types of substrates and barrier layer combinations were considered as shown in Table 1 and schematic switch configurations with various PZT stack designs are depicted in Fig. 3. In the selective transfer process LPCVD grown Si$_3$N$_4$ was chosen as a structural layer whereas for full wafer transfer both Si and PECVD Si$_3$N$_4$ are being investigated. In principle, the choice of a Si$_3$N$_4$/Si substrate offers better tunability of stress-induced pre-bending of PZT cantilever and is also cost-effective as compared to SOI wafers.

Table 1. List of materials for PZT thin film devices

<table>
<thead>
<tr>
<th>Device Layer</th>
<th>Wafer level microdevice distribution</th>
<th>Adhesive full wafer transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>Si</td>
<td>Si and SOI</td>
</tr>
<tr>
<td>Structural Layer</td>
<td>Si$_3$N$_4$ (LPCVD)</td>
<td>Si and Si$_3$N$_4$ (PECVD)</td>
</tr>
<tr>
<td>Diffusion Barrier</td>
<td>TiO$_2$ (RF/DC sputtered &amp; annealed)</td>
<td>TiO$_2$ and SiO$_2$ (Thermal &amp; PECVD)</td>
</tr>
<tr>
<td>Bottom Electrode</td>
<td>Pt/Ti</td>
<td>Pt/Ti</td>
</tr>
<tr>
<td>Functional Layer</td>
<td>PZT, AlN</td>
<td>PZT, AlN</td>
</tr>
<tr>
<td>Top Electrode</td>
<td>Pt/Ti, Au/Cr</td>
<td>Pt/Ti, Au/Cr</td>
</tr>
</tbody>
</table>

Fig. 3. Schematic device design layout

(a) Structural layer (Si/Si$_3$N$_4$) above and below PZT

(b) Cross-sectional layout of a full-wafer transfer-bonded RF switch on the target RF substrate

4. Fabrication - PZT thin film devices

Focusing on devices in which Si$_3$N$_4$ was used as the structural layer, a TiO$_2$ layer was selected as the barrier material - the layer thicknesses used for these were 1.5µm and 30nm respectively. The TiO$_2$ was prepared by RF sputtering of Ti and thermally oxidizing...
at 700°C to obtain the stable rutile phase over the metastable anatase and brookite phases. The RF sputtered bottom Pt/Ti electrodes were patterned or left unpatterned, depending on the design layout for particular transfer bonding scheme, before sol-gel PZT thin films (with Zr/Ti compositions of 30/70) were deposited. The PZT was, therefore, spin-coated onto either a continuous Pt surface or a non-planar mixed surface of TiO₂ and Pt. Following spinning PZT films underwent pyrolysis and crystallization hotplate bakes at 200°C and 530°C respectively.

Finally RF actuators were fabricated by further processing of wafers with PZT microstructure that had been produced by either dry etching (full wafer transfer) or wet etching (selective transfer). The dry etching of PZT stacks is a critical step, since the physical etching of the PZT layer results in sidewall deposits, commonly called “fences”. The problem of fencing could affect the device functionality or fabrication yield and was resolved as described below in section 4.1. PZT was wet-etched in two steps using a solution of (BHF:HCl:NH₄Cl) and followed by HNO₃. Fig. 4 shows successful distribution of a cell of piezo-actuated RF switches using selective transfer bonding technique.

Fig. 4. Distribution of a cell of RF switches

(a) Optical micrograph of the source wafer
(b) SEM image - Transferred devices after release on the receiver using selective transfer bonding

4.1. Plasma etching of PZT microstructure

Although reactive ion etching (RIE) is used extensively for producing fine patterns in PZT e.g. for FeRAMs a limitation has been that with all the currently used etch chemistries (generally F or Cl based) the involatility of some of the etch products often leads to excessive sidewall deposits when a conventional photoresist mask is used. It has been found, however, that fence problems can be alleviated by hard masking and good results have been achieved recently in the fabrication of FeRAM devices, for example, using TiN and TiO₂ masks [8]. The sputtered Ni has also been a popular choice due to its extremely low RIE etch rate but a low film stress, another key requirement in view of the often observed low adhesion of layers deposited on top of PZT, is difficult to obtain with this material. Consequently, following the work of Subasinghe on bulk PZT [9], a low stress electroplated Ni hard-mask process has been developed to provide good stopping on the underlying thin Pt electrode. An example of the heavy sidewall deposits produced by this process when conventional photoresist masking is used is shown in Fig. 5 (a). Ni etches at a much lower rate than the PZT (etch selectivity ~8:1) making it an ideal etch mask. Ni thicknesses in the range 0.5-1µm are used to etch up to 1µm thick PZT stacks although thinner layers could be used. Following PZT etching the Ni is removed in a FeCl₃ solution to leave fence free features with steep side walls (~63°) as shown in Fig.5 (b).

Fig. 5. SEM micrographs of etched PZT stacks

(a) Sidewall deposits during dry etching when using a photoresist mask; (b) Fence-free etched profile when electroplated Ni hard mask used instead.

4.2. PZT microstructure evaluation

The surface morphology of PZT microstructures was analyzed using AFM method. The state of the surface underneath the Pt/Ti electrodes and TiO₂ barrier layer strongly influences PZT thin film growth and so for example Pt hillock formation during PZT crystallization must be avoided to ensure a smooth texture with lower surface roughness [10]. A thermally stable electrode and barrier interface must be achieved prior to depositing PZT and key to this is complete oxidation of the Ti so as to prevent delamination by Pt hillock formation a well known effect that occurs due to increased compressive stress during high temperature annealing. Fig. 6 (a) exhibits AFM image of a high quality PZT film with dense texture (surface roughness ~0.7nm). In contrast Fig. 6 (b) shows a blistered PZT surface as evidence of Pt hillocks formed on the relatively flat PZT grains.

Fig. 6. Surface morphology of PZT on Pt/TiO₂/Si₃N₄

AFM images illustrate (a) high quality PZT thin film and (b) Pt hillocks on a blistered PZT surface

It has been found with all the different layer structures investigated that the (111) PZT perovskite grain orientation dominates. This can be seen clearly for example in the XRD spectra depicted in Fig. 7 revealing the fact that the PZT on Pt/TiO₂/Si₃N₄ structures also exhibit a less preferred (110) orientation unlike PZT/Pt/Ti/SiO₂ structures. However the higher peak intensity of the preferred perovskite (111) phase
that high quality PZT thin films can be grown on top of PZT composites. The experimental results established which is consistent with results obtained from standard longitudinal piezoelectric coefficient, \(d_{33,f}\) of the PZT using laser scanning vibrometry and the effective stacks before and after poling of a PZT composite on TiO\(_2\)/Si\(_3\)N\(_4\). The saturation poled devices were 41\(\mu\)C/cm\(^2\), 29\(\mu\)C/cm\(^2\) and 78kV/cm polarization, remnant polarization and coercive field respectively, establishing that the films had fully crystallized in the perovskite phase.

**4.3. Piezoelectric thin film properties**

Electrical characterization was carried out to assess the dielectric properties and polarization hysteresis of the PZT films. The measurements were conducted on PZT thin film capacitors composed of various layer designs and Cr/Au evaporated dots as top electrode. The measured values of the dielectric constant were 378 and 314 and the loss tangent as 0.02 and 0.025 at 100 kHz, before and after poling respectively. The parameters obtained from different materials exhibit only ~10% variation in capacitance values and have very low loss compared to standard materials exhibit only ~10% variation in capacitance values and have very low loss compared to standard PZT stacks on SiO\(_2\)/Si. Fig. 8 shows hysteresis loops of a PZT composite on TiO\(_2\)/Si\(_3\)N\(_4\). The saturation polarization, remnant polarization and coercive field in poled devices were 41\(\mu\)C/cm\(^2\), 29\(\mu\)C/cm\(^2\) and 78kV/cm respectively, establishing that the films had fully crystallized in the perovskite phase.

**5. Conclusions**

Layer designs for devices incorporating PZT thin films have been formulated which feature thermally stable barrier/electrode interfaces combined with suitable process layouts that are compatible with transfer bonding techniques (developed within the Q2M project) for wafer-scale integration of piezo-actuated RF MEMS switches and components. The surface morphology and the electrical properties of PZT microstructures were assessed to understand material constraints imposed by the choice of different layers. A new low stress electroplated Ni hard mask process was developed to establish fence-free patterning of PZT stacks during plasma etching of full wafer transferred cantilever beams. The first successful distribution of PZT-based RF actuators using selective transfer bonding has been demonstrated.

**Acknowledgements**

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**References**

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